IN THE CLAIMS:

Amend claim 2 as follows:

B4

--2. (amended) The channel region as claimed in claim 1, wherein said semiconductor region comprises a well region of the second conductivity type selectively provided in a semiconductor substrate of the first conductivity type.--

Amend claim 5 as follows:

B5

--5. (amended) The well region as claimed in claim 4, wherein said upper surface of said impurity diffused region is bounded with a gate insulating film.--

✓Cancel claims 6-7.

Amend claim 11 as follows:

B6

--11. (amended) A semiconductor wafer including:

an impurity diffused region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type; and

an oxide film overlying said impurity diffused region with an upper surface of the semiconductor region being exposed at an upper surface of said semiconductor wafer on each end of the oxide film,

wherein an interface of said impurity diffused region to said oxide film lies at a lower level than the upper surface of said semiconductor wafer.--

Amend claim 12 as follows:

--12. (amended) The semiconductor wafer as claimed in claim 11, wherein said semiconductor region comprises a well region of the second conductivity type selectively provided in a semiconductor substrate of the first conductivity type.--

B7

Add the following new claims:

--27. (new) The well region as claimed in claim 4, wherein said impurity diffused region forms a channel layer of said depletion type lateral field effect transistor.

B8

--28. (new) A semiconductor wafer comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer of the first conductivity type overlying said semiconductor substrate;

a well region of a second conductivity type selectively provided in said epitaxial layer; and

an impurity diffused channel region being selectively provided in said well region, and said impurity diffused channel region being doped with an impurity of the first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor,

wherein said upper surface of said impurity diffused channel region lies at a lower level than said upper surface of said well region.

--29. (new) The semiconductor wafer as claimed in claim

28, wherein said upper surface of said impurity diffused region is bounded with a gate insulating film.

--30. (new) The depletion type lateral MOS field effect transistor of claim 8, wherein,

the channel region, provided in the semiconductor region, comprises throughout the channel region a first concentration of first impurities of the second conductivity type and a higher second concentration of second impurities of the first conductivity type whereby the channel region is of the first conductivity type, and

B8 Cont.

the semiconductor region comprises a third concentration of the first impurities of the second conductivity type, the third concentration being higher than the first concentration.

--31. (new) The channel region of claim 1, wherein,

the channel region, provided in the semiconductor region, comprises a first concentration of first impurities of the second conductivity type and a higher second concentration of second impurities of the first conductivity type whereby the channel region is of the first conductivity type, and

the semiconductor region comprises a third concentration of the first impurities of the second conductivity type, the third concentration being higher than the first concentration.

--32. (new) The well region of claim 4, wherein,

the impurity diffused region is a channel region,

the channel region comprises a first concentration of a first impurity of the second conductivity type and a higher second concentration of the impurity of the first conductivity type whereby the channel region is of the first conductivity type, and

the well comprises a third concentration of the first impurity of the second conductivity type, the third concentration being higher than the first concentration.

B8 Cont.

--33. (new) A depletion type lateral field effect transistor, comprising:

an n+-type semiconductor substrate (1) with a first impurity concentration;

an $n^-$-type epitaxial layer (2) with a second, impurity concentration formed over the substrate, the second concentration being lower than the first concentration;

a p-well region (5) formed in the $n^-$-type epitaxial layer with an uppermost surface of the p-well region being co-planar with an uppermost surface of the $n^-$-type epitaxial layer; and

an n-type channel region (6) formed in the p-well region; and

wherein an uppermost surface of the channel region lies at a lower level than the uppermost surface of the p-well region.

--34. (new) The transistor of claim 33, further comprising:

a gate oxide film extending over the channel region;

field oxide films contacting each end of the gate oxide film and extending over the p-well;

a source region contacting a first end of said channel region, said gate oxide film, and one of said field oxide films; and

a drain region contacting a second end of said channel region, said gate oxide film, and another of said field oxide films.

B8 cont.

--35. (new) The transistor of claim 33, wherein,

the gate oxide film extending over the channel region the n-type channel region comprises a low concentration of a p-type impurity and a higher concentration of an n-type impurity, and

the p-well region comprises the p-type impurity.

--36. (new) The transistor of claim 35, wherein a concentration of the p-type impurity in the p-well is higher than the low concentration of the p-type impurity in the n-type channel region.

--37. (new) The transistor of claim 34, wherein,

the gate oxide film extending over the channel region has a thickness of 300 angstroms, and

the field oxide films contacting each end of the gate oxide film have a thickness of at least 5000 angstroms.

--38. (new) The channel region as claimed in claim 2, wherein said well region comprises a planar lower surface along an entire length of the lower surface.

--39. (new) The well region of claim 4, wherein said well region comprises a planar lower surface along an entire length of the lower surface.

--40. (new) The semiconductor wafer as claimed in claim 12, wherein said well region comprises a planar lower surface along an entire length of the lower surface.--

REMARKS

The application has been amended to be in condition for allowance at the time of the next Official Action.

Claims 1-5, 8-14, and 27-40 are present.

Support for claims 30-32 can be found at least in the disclosure spanning pages 15-16 of the specification; page 19; and Figures 2A-2C.

The Official Action rejected claims 5-7 under §112, second paragraph, as indefinite. The Official Action also noted that there were two claims originally filed as claim 6.

Claim 5 has been amended to depend from claim 4, thereby remedying the noted antecedent basis problem.

Claims 6-7 have been cancelled and added as new claims